Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit comprising:

a sense amplifier;

first and second bitlines coupled to the sense amplifier;

a plurality of memory cells coupled to the sense amplifier, during a memory access, a selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier; and

a test circuit coupled to the bitlines, the test circuit, when activated, varies the magnitude of the differential read signal differential read signal by varying the capacitance on at least one of the bitlines.

2. (currently amended) ~~The~~ An integrated circuit ~~of claim 1~~ comprising:

a sense amplifier;

first and second bitlines coupled to the sense amplifier;

a plurality of memory cells coupled to the sense amplifier, wherein the memory cells comprise 2T2C memory cells, during a memory access, a selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier; and

a test circuit coupled to the bitlines, the test circuit, when activated, varies the magnitude of the differential read signal.

3. (currently amended) ~~The~~ An integrated circuit ~~of claim 1~~ comprising:

a sense amplifier;

first and second bitlines coupled to the sense amplifier;

a plurality of memory cells coupled to the sense amplifier, wherein the memory cells comprise 2T2C ferroelectric memory cells, during a memory access, a selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier; and

a test circuit coupled to the bitlines, the test circuit, when activated, varies the magnitude of the differential read signal.

4. (currently amended) The integrated circuit of claim ~~1~~ 2 wherein a first read signal is provided on the first bitline and a second read signal is provided on the second bitline during a memory access of one memory cell on the bitline pair, the first and second read signal forms the differential read signal, where one of the first or second read signal is equal to V_{LO} and the other is V_{HI}.

5. (original) The integrated circuit of claim 4 wherein the test circuit comprises:

a first test capacitor having first and second terminals, the first terminal coupled to a first test input terminal and the second terminal coupled to the first bitline; and

a second test capacitor having first and second terminals, the first terminal coupled to a second test input terminal and the second terminal coupled to the second bitline.

6. (original) The integrated circuit of claim 5 wherein a first active test signal at the first test input terminal increases the magnitude of the first read signal.

7. (original) The integrated circuit of claim 5 wherein a second active test signal at the second test input terminal increases the magnitude of the second read signal.

8. (original) The integrated circuit of claim 5 wherein an active test signal is provided at either the first or second test input terminal to increase the magnitude of the first or second read signal.

9. (original) The integrated circuit of claim 8 wherein the magnitude of the read signal equal at V_{LO} is increased to reduce the differential read signal.

10. (original) The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is between V_{LO} and V_{HI}.

11. (original) The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is equal to about half way between V_{LO} and V_{HI}.

12. (original) The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is equal to about one third between V_{LO} and V_{HI}.

13. (original) The integrated circuit of claim 9 wherein the increase in magnitude of the read signal depends on the capacitance of the test capacitor and magnitude of the active test signal.

14. (original) The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is between V_{LO} and V_{HI}.

15. (original) The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is equal to about half way between V_{LO} and V_{HI}.

16. (original) The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest}, where V_{LOTest} is equal to about one third between V_{LO} and V_{HI}.

17. (currently amended) The integrated circuit of claim 4 wherein the test circuit comprises:

a first set of x test capacitors having first terminals coupled to respective first input test signals and ~~the~~ second terminals coupled to the first bitline; and

a second set of y test capacitors having first terminals coupled to respective second input test signals and second terminals coupled to the second bitline.

18. (original) The integrated circuit of claim 17 wherein the capacitors within the first set have different values and the capacitors within the second set have different values.

19. (currently amended) The integrated circuit of claim 18 wherein the first set of test capacitors can vary the first read signal by 2^x-1 levels and the second set of test capacitors can vary the read signal by 2^y-1 levels.

20. (original) The integrated circuit 19 of claim wherein x = y.

21. (new) The integrated circuit of claim 1 wherein the test circuit comprises:

a first set of x test capacitors having first terminals coupled to respective first input test signals and second terminals coupled to the first bitline; and

a second set of y test capacitors having first terminals coupled to respective second input test signals and second terminals coupled to the second bitline.

22. (new) The integrated circuit of claim 21 wherein the first set of test capacitors can vary the first read signal by 2^x-1 levels and the second set of test capacitors can vary the read signal by 2^y-1 levels.

23. (new) The integrated circuit of claim 22 wherein the differential read signal includes first and second read signals on first and second bitlines, where one of the first or second read signal is equal to V_{LO} and the other is V_{HI} and the magnitude of the differential read signal is varied by increasing the magnitude of V_{LO} to V_{LOTest}, where V_{LOTest} is between V_{LO} and V_{HI}.

24. (new) An integrated circuit comprising:

a sense amplifier;

first and second bitlines coupled to the sense amplifier;

a plurality of memory cells coupled to the sense amplifier, during a memory access, a selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier, the differential read signal includes first and second read signals on first and second bitlines, where one of the first or second read signal is equal to V_{LO} and the other is V_{HI}; and

a test circuit coupled to the bitlines, the test circuit, when activated, varies the magnitude of the differential read signal differential read signal.

25. (new) A method of operating an integrated circuit comprising:

providing the IC with a sense amplifier coupled to first and second bitlines having a plurality of memory cells coupled thereto, wherein when one memory cell is selected for a read access, the selected memory cell produces a differential read signal on the bitlines for sensing by the sense amplifier; the differential read signal indicating a first or a second state being stored in the selected memory cell, the differential read signal includes a first read signal provided on the first bitline and a second read signal provided on the second bitline of the bitline pair, where one of the first or second read signal is equal to V_{LO} and the other is V_{HI}; and

activating a test circuit coupled to the bitlines during test mode to vary the magnitude of the differential read signal by varying the capacitance on at least one of the bitlines.